IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application for:

Steven Teig

Serial No.: 09/733,104

Filing Date: 12/07/2000

For: MULTI-DIRECTIONAL WIRING ON A SINGLE METAL LAYER

Examiner: Chu, Chris C.

Group Art Unit: 2815

SUPPLEMENTAL APPEAL BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief is filed in response to the Examiner's October 27, 2003 Response to Applicants' Appeal Brief. In the October 27, 2003 response, the Examiner presented Applicants with the option of either filing a reply under 37 CFR 1.111 to the Examiner's new ground for rejection which was supported by a new prior art reference or requesting reinstatement of the appeal. In accordance with 37 CFR 1.193(b)(2), Applicants hereby request reinstatement of the appeal. Please charge any additional fees or credit any overpayment to Deposit Account No. 501128.

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Cadence Design Systems, a Delaware Corporation, having its principal place of business in San Jose, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignees thereof.

III. STATUS OF CLAIMS

Claims 1-17 are pending in the present application. Applicants have successfully traversed each of the Examiner's drawing objections and claim rejections. Claims 1-17 are in condition for allowance.

IV. STATUS OF AMENDMENTS

No amendments to the application were submitted after final rejection.

V. SUMMARY OF INVENTION

The claims (claims 1-16 and 17) are directed towards an integrated circuit having at least one metal layer that includes conductors to provide interconnectivity for the integrated circuit chip. For purposes of assigning preferred wiring directions for the conductors, the metal layer is divided into at least two sections (e.g., first section and second section). *Specification, page 2, lines 15-16.* Each section contains at least one thousand wires (*i.e.*, conductors) to interconnect points on the integrated circuit. *Specification, page 2, lines 16-17.* The conductors in each section are oriented in a preferred direction relative to the boundaries of the integrated circuit chip. A "preferred direction" is a direction in which at least fifty percent of the conductors are oriented. *Specification, page 2, lines 17-20.* **Figure 10** illustrates an example metal layer with multiple preferred directions.

The first and second sections of the claimed integrated circuit have different preferred wiring directions. One of the sections has a preferred wiring direction that is diagonal. A diagonal direction is neither vertical nor horizontal. Examples of diagonal directions include octalinear (*i.e.*, plus or minus 45 degrees from vertical or horizontal) and hexalinear (*i.e.*, plus or minus 30 or 60 degrees from vertical or horizontal). *Specification, page 3, lines 4-8; see also, page 6, lines 12-16.* **Figure 1b** illustrates an example of an integrated circuit that employs diagonal wiring. Furthermore, one of the sections contains at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in a diagonal wiring direction. *See, for example,* ***Figure 14***. A "Manhattan direction" is either vertical or horizontal. *Specification, page 3, lines 4-6.* **Figure 6a** illustrates an embodiment for a legacy Manhattan metal layer configuration.

VI. ISSUES

I. Whether the subject claims are unpatentable under 35 U.S.C. § 112, first paragraph, as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

II. Whether the drawings of the application disclosed every feature of the invention specified in the claims under 37 CFR 1.83(a).

III. Whether the subject claims are unpatentable under 35 U.S.C. § 103(a) over Juengling (U.S. Pat. No. 6,448,591) and Rostoker (U.S. Pat. No. 5,650,653).

IV. Whether the subject claims are unpatentable under 35 U.S.C. § 103(a) over Jones (U.S. Pat. No. 5,980,093).

VII. GROUPING OF THE CLAIMS

Applicants contend that all of the pending claims (1-17) stand or fall together. Accordingly, Applicants are not grouping the claims on appeal.

VIII. ARGUMENT

In view of Applicants' Appeal Brief and a January 5, 2004 interview with both the Examiner and a Master's Level Patent Examiner (An Interview Summary signed by the Master's Level Patent Examiner is attached to this Supplemental Appeal Brief), all of claims 1-17 are in condition for allowance.

A. Applicants Appeal Brief Successfully Traversed the Examiner's Final Office Action rejection of claims 1-17 under 35 U.S.C. § 103(a) as obvious over Juengling and Rostoker.

On June 3, 2003, Applicants filed an Appeal Brief in response to the Examiner's September 26, 2002 Final Office Action. Applicants' Appeal Brief presented arguments which overcame both the Examiner's Final Office Action rejection of claims 1-9, 11, and 13-17 as obvious over Juengling and the Examiner's Final Office Action rejection of claims 10 and 12 as obvious over Juengling in view of Rostoker. In response to Applicants' Appeal Brief, the Examiner reopened prosecution with a new non-final Office Action dated October 27, 2003.

B. During a January 5, 2004 Interview, Applicants Successfully Presented Arguments Which Overcame the Drawing Objections and Claim Rejections the Examiner Asserted in the New October 27, 2003 Non-final Office Action.

The Examiner's new non-final October 27, 2003 Office Action repeated both the drawing objections and the 35 U.S.C. § 112, first paragraph rejections from the Final Office Action, but presented a new 35 U.S.C. § 103(a) rejection. The Examiner's new rejection asserted that claims 1-

17 are obvious under 35 U.S.C. § 103(a) over Jones. After receiving the October 27, 2003 Office Action, Applicants requested and obtained an Interview with the Examienr and a Master's Level Patent Examiner. Applicants appreciate both the Examiner's and the Master's Level Patent Examiner's willingness to conduct an Interview regarding the objections and rejections included within the new October 27, 2003 Office Action. Applicants further appreciate the Master's Level Patent Examiner's acknowledgment that, during the Interview, Applicants presented arguments which appear to overcome the drawing objections; the 35 U.S.C. § 112, first paragraph rejections; and the Jones reference.

However, Applicants respectfully disagree with the Master's Level Patent Examiner's assertion that the appropriate next step in this case is to reopen prosecution and thus require Applicants to respond to the results of a new search. Applicants have already successfully traversed rejections of claims 1-17 in three separate Office Actions. In addition to retaining counsel to respond to these three Office Actions, Applicants have retained counsel to draft and file both an Appeal Brief and the current Supplemental Appeal Brief. Applicants should not now be required to retain counsel to respond to the two more Office Actions which will probably result from a new search. The Examiner has already had several opportunities to review the patentability of claims 1-17 and has been unable to cite any prior art which calls the patentability of these claims into question. Continuing to prosecute claims 1-17 at this point in this case is an inefficient use of U.S.P.T.O. and Applicants' resources.

IX. CONCLUSION

Because Applicants have overcome the objections and rejections in both the Final Office Action which is the subject of this appeal and the objections and rejections in the non-Final Office Action which the Examiner used to reopen prosecution after Applicants overcame the objections and rejections in the Final Office Action, Applicants respectfully submit that the drawings fully comply with all appropriate rules and that claims 1-17 are in condition for allowance. Accordingly, Applicants hereby request that the Board 1) overturn the Examiner's drawing objections and claim rejections and 2) direct that a Notice of Allowance be issued in this case. Prompt allowance of the present application is earnestly solicited.

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APPENDIX

The following claims are the subject of this Appeal.

1. An integrated circuit comprising:

at least one metal layer comprising a plurality of sections, each section comprising at least one thousand conductors situated in a contiguous area to interconnect points on the integrated circuit, wherein a preferred direction, within a section, defines a direction, relative to the boundaries of the integrated circuit, for at least fifty percent of conductors in the section;

a first section comprising a first preferred direction for the conductors deposed in the first section; and

a second section comprising a preferred diagonal wiring direction for the conductors deposed in the second section, such that the diagonal wiring preferred direction is a direction different from the first preferred direction, said second section further comprising at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in said preferred diagonal wiring direction.

2. The integrated circuit as set forth in claim 1, wherein the first preferred direction comprises a diagonal direction.

3. The integrated circuit as set forth in claim 2, wherein the first preferred diagonal direction comprises a direction perpendicular to said preferred diagonal wiring direction in said second section.

4. The integrated circuit as set forth in claim 1, wherein the diagonal direction comprises an octalinear direction.

5. The integrated circuit as set forth in claim 1, wherein the diagonal direction comprises a hexalinear direction.

6. The integrated circuit as set forth in claim 1, wherein:

the first preferred direction comprises a first diagonal direction; and

the second preferred direction comprises a second diagonal direction, different from the first diagonal direction.

7. The integrated circuit as set forth in claim 6, wherein:

the first diagonal direction comprises an octalinear direction; and

the second diagonal direction comprises an octalinear direction complementary to the first diagonal direction.

8. The integrated circuit as set forth in claim 6, wherein:

the first diagonal direction comprises a hexalinear direction; and

the second diagonal direction comprises a hexalinear direction complementary to the first diagonal direction.

9. The integrated circuit as set forth in claim 6, wherein:

The first diagonal direction comprises an octalinear direction; and

The second diagonal direction comprises a hexalinear direction.

10. The integrated circuit as set forth in claim 1, further comprising at least one more additional section having a preferred direction comprising a diagonal direction.

11. The integrated circuit as set forth in claim 1, further comprising at least one more section having a preferred direction comprising a Manhattan direction.

12. The integrated circuit as set forth in claim 1, further comprising at least one additional wire deposed in a section with a direction different than the preferred direction of the section.

13. The integrated circuit as set forth in claim 12, wherein:

the preferred direction comprises a diagonal direction; and

the direction different than the preferred direction comprises a Manhattan direction.

14. The integrated circuit as set forth in claim 13, wherein:

the preferred direction comprises a diagonal direction; and

the direction different than the preferred direction comprises a Manhattan direction.

15. The integrated circuit as set forth in claim 13, wherein:

the preferred direction comprises a Manhattan direction; and

the direction different from the preferred direction comprises a diagonal direction.

16. The integrated circuit as set forth in claim 13, wherein the direction different than the preferred direction comprises a direction complementary to the preferred direction.

17. An integrated circuit comprising:

at least one metal layer comprising a plurality of sections, each section comprising at least one thousand conductors situated in a contiguous area to interconnect points on the integrated circuit, wherein a preferred direction, within a section, defines a direction, relative to the boundaries of the integrated circuit, for at least fifty percent of conductors in the section;

a first section comprising a Manhattan wiring direction for the conductors deposed in the

first section, the first section further comprising at least one conductor deposed in a diagonal direction coupled to a conductor deposed in the Manhattan wiring direction; and

a second section comprising a preferred diagonal wiring direction for the conductors deposed in the second section, such that the diagonal wiring preferred direction is a direction different from the first preferred direction.